

Si4420DY

N-channel enhancement mode field-effect transistor

Rev. 01 — 28 May 2001

Product data

1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

Si4420DY in SOT96-1 (SO8).

2. Features

- Low on-state resistance
- Fast switching
- TrenchMOS™ technology.

3. Applications

- DC to DC convertors
- DC motor control
- Lithium-ion battery applications
- Notebook PC
- Portable equipment applications.

4. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	Top view MBK187 SOT96-1 (SO8)	MBB076
4	gate (g)		
5,6,7,8	drain (d)		

1. TrenchMOS is a trademark of Royal Philips Electronics.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	30	V
I_D	drain current (DC)	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	12.5	A
P_{tot}	total power dissipation	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	2.5	W
T_j	junction temperature		–	150	°C
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 12.5$ A	7.3	9	mΩ
		$V_{GS} = 4.5$ V; $I_D = 10.5$ A	10.9	13	mΩ

6. Limiting values

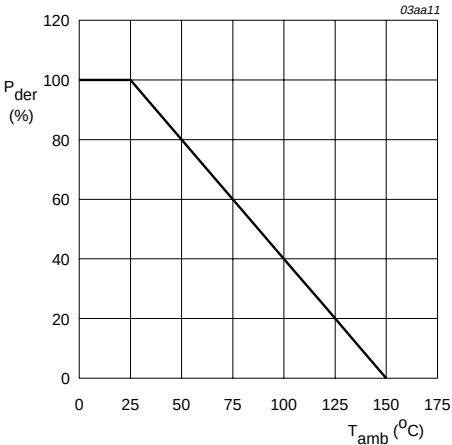
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s; Figure 2 and 3	–	12.5	A
		$T_{amb} = 70$ °C; pulsed; $t_p \leq 10$ s; Figure 2	–	10	A
I_{DM}	peak drain current	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	50	A
P_{tot}	total power dissipation	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s;	–	2.5	W
		$T_{amb} = 70$ °C; pulsed; $t_p \leq 10$ s; Figure 1	–	1.6	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

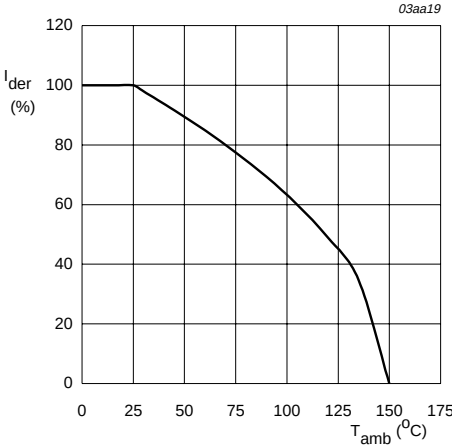
Source-drain diode

I_S	source (diode forward) current (DC)	$T_{amb} = 25$ °C; pulsed; $t_p \leq 10$ s	–	2.3	A
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

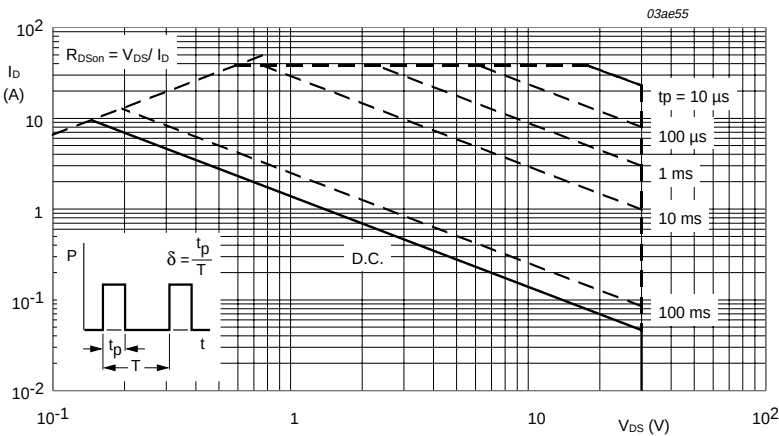
Fig 1. Normalized total power dissipation as a function of ambient temperature.



$V_{GS} \geq 10\text{ V}$

$$I_D = \frac{I_{D(25^{\circ}C)}}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



$T_{amb} = 25\text{ }^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint, $t \leq 10$ sec. Figure 4	50	K/W

7.1 Transient thermal impedance

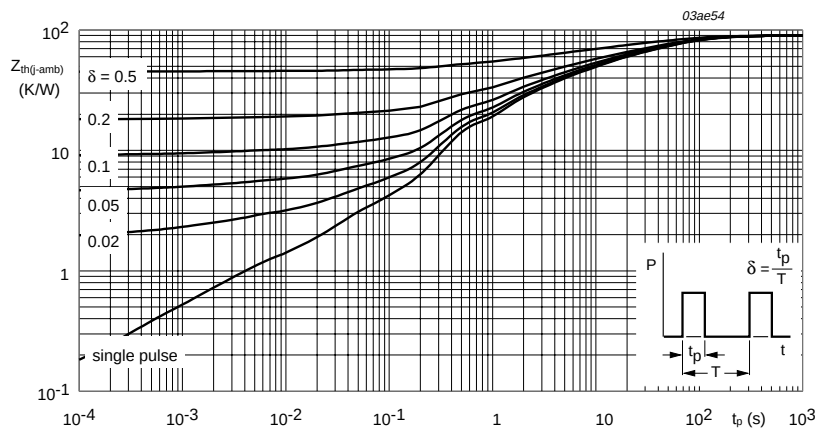


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; Figure 9	1	–	–	V
I _{DSS}	drain-source leakage current	V _{DS} = 30 V; V _{GS} = 0 V				
		T _j = 25 °C	–	–	1	μA
		T _j = 55 °C	–	–	5	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	–	–	100	nA
I _{D(on)}	on-state drain current	V _{DS} ≥ 5 V; V _{GS} = 10 V	30		–	A
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 12.5 A; Figure 7 and 8	–	7.3	9	mΩ
		V _{GS} = 4.5 V; I _D = 10.5 A; Figure 7 and 8	–	10.9	13	mΩ
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 15 V; I _D = 7 A; Figure 11	–	15	–	S
Q _{g(tot)}	total gate charge	I _D = 12.5 A; V _{DD} = 15 V; V _{GS} = 10 V; Figure 14	–	64.5	120	nC
Q _{gs}	gate-source charge		–	7.6	–	nC
Q _{gd}	gate-drain (Miller) charge		–	11.5	–	nC
t _{d(on)}	turn-on delay time	V _{DD} = 15 V; R _D = 15 Ω; V _{GS} = 10 V; R _G = 6 Ω	–	12	30	ns
t _r	turn-on rise time		–	15	60	ns
t _{d(off)}	turn-off delay time		–	60	150	ns
t _f	turn-off fall time		–	50	140	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 2.3 A; V _{GS} = 0 V; Figure 13	–	0.7	1.1	V
t _{rr}	reverse recovery time	I _S = 2.3 A; dI _S /dt = –100 A/μs	–	60	–	ns

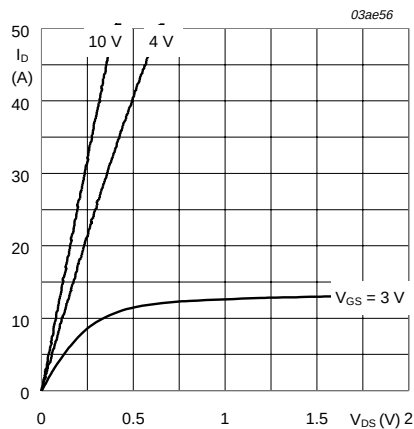


Fig 5. Output characteristic; drain current as a function of drain-source voltage; typical values.

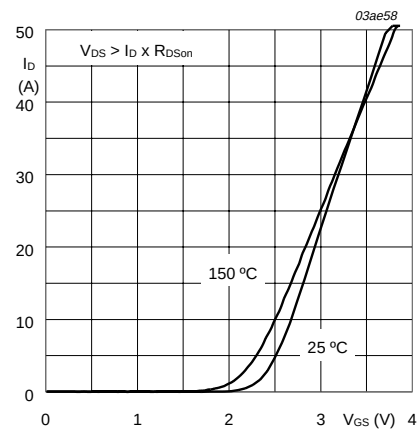
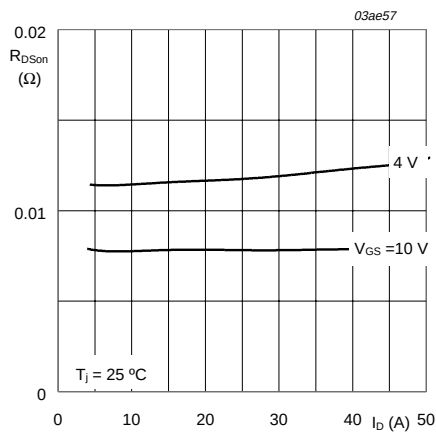
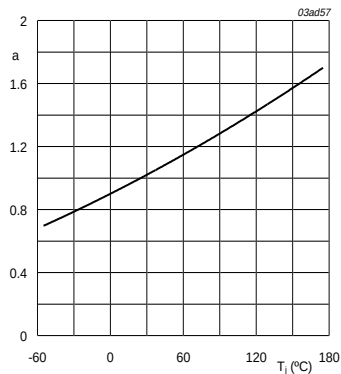


Fig 6. Transfer characteristic: drain current as a function of gate-source voltage; typical values



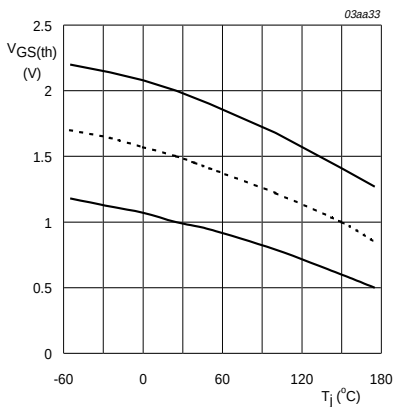
$T_J = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



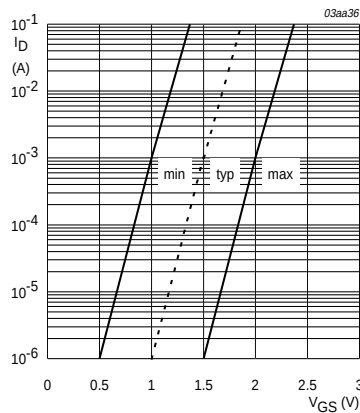
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



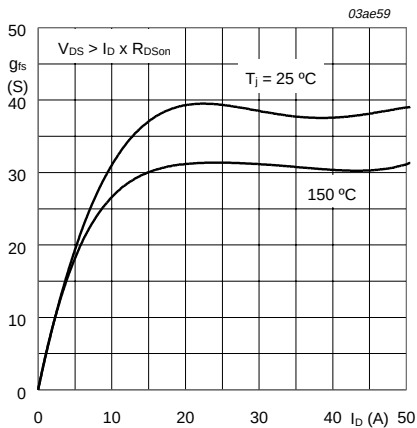
$I_D = 250\text{ }\mu\text{A}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



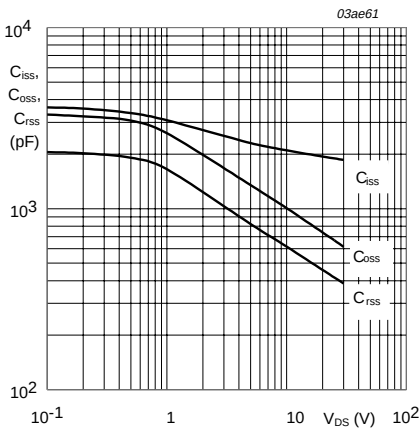
$T_J = 25^\circ\text{C}$; $V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



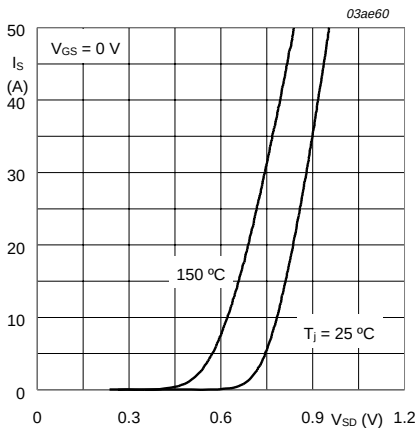
$T_j = 25\text{ }^{\circ}\text{C}$ and $150\text{ }^{\circ}\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 11. Forward transconductance as a function of drain current; typical values.



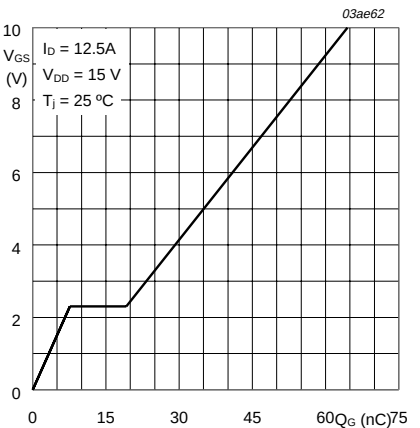
$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^{\circ}\text{C}$ and $150\text{ }^{\circ}\text{C}$; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



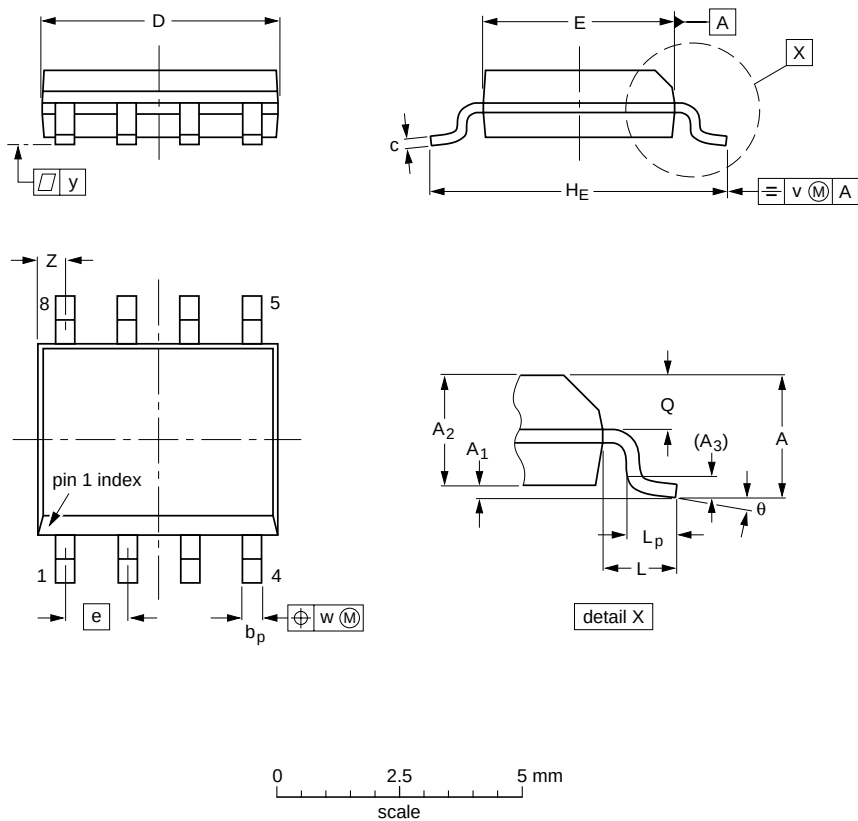
$I_D = 12.5\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				97-05-22- 99-12-27

Fig 15. SOT96-1 (SO8).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010528	-	Product specification; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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